Real-Time and Embedded Systems Development based on Discrete Event Modeling and Simulation

By

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A thesis submitted to the Faculty of Graduate and Postdoctoral Affairs

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Electrical and Computer Engineering

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The undersigned recommend to

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acceptance of the thesis

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Abstract

The design and development of embedded hard real-time (RT) systems is one of the most complex software development practices, because of the criticality and timeliness required for these systems. One critical aspect of RT systems is the production of outputs before the specified deadline. A late output caused by an overrun condition in the processing of RT tasks, not only degrades the system performance but also produces catastrophic results. Formal methods are promising alternatives in dealing with the design issues of these applications, however they do not scale well for complex systems. A cost-effective approach to verify the design and implementation details of such applications is the use of Modeling and Simulation (M&S). These methods provide dynamic and risk-free testing environments to verify different variable scenarios. M&S is now limited to feasibility analysis and verification of such systems, hence the simulation models are not used in the development of the final embedded application.

This dissertation is proposing an M&S-based method referred to as DEVSRT (Discrete EVent System Specifications in Real-Time) to solve the discontinuity between the simulation models and the final embedded software. The proposed approach combines the advantages of a simulation-based method and a formal methodology to develop embedded applications, and integrate simulation models with hardware components.

The research also proposes an integration of DEVSRT with Imprecise Computations theory. The proposed I-DEVS (imprecise DEVS) formalism uses a dynamic scheduling algorithm based on the criticality of the RT tasks to manage overload situations in the system by degrading the system's output accuracy in order to meet hard deadlines. The algorithm detects transient overloading conditions early enough to carry out a proper imprecise scheduling of RT tasks, providing a more reliable runtime platform.